

Description

Forming Shallow Trench Isolation Without the Use of CMP

BACKGROUND OF INVENTION

[0001] TECHNICAL FIELD

[0002] The field of the invention is that of forming shallow trench isolation structures (STI) separating components of an integrated circuit with insulating films that are deposited in shallow trenches.

[0003] BACKGROUND OF THE INVENTION

[0004] In recent years, the LOCOS method of forming isolation structures has given way to a shallow trench isolation method in which a trench is etched directionally into the semiconductor substrate.

[0005] The etching process permits much better control of the lateral extent of the structure than was possible with the LOCOS method, since the oxygen used in the oxidizing step diffused laterally and extended outward from the

aperture in the hard mask defining the intended extent of the isolation structure.

[0006] The trench isolation process conventionally uses chemical-mechanical polishing (CMP) in which an abrasive removes excess trench fill material to establish a planar surface.

[0007] A drawback of this approach is that the CMP process produces scratches or chatter marks in the surface that may contribute to the total number of defects.

[0008] In current technology, one of the highest yield detractors in front end processing is CMP-induced defects.

[0009] Typical "fixed abrasive" CMP processes leave a high density of scratches. Slurry CMP produces "dishing" or local nonuniformity in wide isolation areas.

[0010] In addition, scratches may be filled with insulator or conductor, both of which can cause device failure or inconsistent performance.

[0011] The mechanical abrasive process tends to produce substantial variation in planarity over the wafer surface.

[0012] In addition, the equipment required and consumables for the process, such as slurry and abrasive pads, contribute to the cost of chips fabricated using this technique.

[0013] U.S. Patent 6,001,696 shows a method of filling isolation

apertures completely up to the top of a thick lift-off layer, with the result that there is a tall projection stub on the top of the isolation members, extending to a considerable distance above the device layer that may interfere with the lowest level of interconnect, such as a polysilicon local interconnect.

[0014] The semiconductor industry could benefit from a technique that produces acceptable planarity without the defects, extra equipment, consumable cost, and cycle time associated with the CMP process.

SUMMARY OF INVENTION

[0015] The invention relates to a method of filling and planarizing shallow trench isolation that does not employ CMP.

[0016] The inventive method comprises depositing a pad insulator layer of an appropriate thickness to set the isolation height, patterning the isolation trenches and depositing nonconformal trench fill material such that the amount of trench fill material deposited on the interior walls of the trench aperture is less than the amount of material within the trench. The trench fill material is recessed to expose the sidewalls of the pad insulator. The active areas without isolation trenches are treated to remove the pad layer.

[0017] One feature of the invention is that the pad insulator layer

may be implanted to increase the etch rate relative to the etch rate of the trench fill material and facilitate removal.

[0018] Another feature of the invention is the formation of supplementary field apertures that break up large expanses of pad insulator.

BRIEF DESCRIPTION OF DRAWINGS

[0019] Figure 1 illustrates a sequence in a first embodiment of the invention.

[0020] Figure 2 illustrates a sequence in an embodiment employing supplementary field apertures.

[0021] Figure 3 illustrates a sequence in an embodiment employing ion implantation.

DETAILED DESCRIPTION

[0022] Figure 1 illustrates a sequence of steps in a method according to the invention. The starting material in Figure 1A is a silicon substrate 5 having a buried oxide insulator (BOX) 10 formed in it with a silicon device layer 20 above and over the BOX (SOI). As used herein, "above" means higher than or further from the substrate. When applicable, terms such as over or directly above will be used in indicate that one element is vertically directly over another element in a cross sectional view. Pad oxide 30 has been

formed on the wafer, and pad nitride 40, having a thickness selected as discussed below, completes the structure.

[0023] Figure 1B shows the result of etching a number of apertures 110 through the pad nitride and pad oxide and then forming a trench through device layer 20 and stopping on the top surface of BOX 10. The trench may extend into the box, as a result of process variations. The width of the trench is set by functional considerations, well known to those skilled in the art. The trench will be filled with an insulator, and its function is to isolate adjacent devices from one another. The depth and width will be set to accomplish that function.

[0024] The invention may be applied to bulk semiconductor wafers, such as silicon or germanium as well as to SOI wafers or any semiconductor on insulator wafers. In the case of bulk wafers, the term device layer refers to the top level (which need not be a separate layer) of semiconductor material in which the devices are formed.

[0025] Figure 1C shows the result of partially filling apertures 110 with an isolation insulator 150. At the stage illustrated, the insulating material has just risen to the level of the top of device layer 20. A relatively thin layer of isola-

tion insulator material 150 (trench fill) has formed on the vertical walls of the apertures and on the top of the pillars of nitride 40 that are between neighboring trenches.

[0026] The deposition technique of isolation insulator 150 is preferably chosen to reduce the amount of material attached to the trench walls because that material is to be removed in subsequent steps. It is desirable that the thickness on the walls be less than a threshold amount in order to facilitate exposure of the pad nitride walls in the subsequent removal step. High density plasma (HDP) enhanced CVD of oxide (silicon dioxide) is a preferred method that deposits the material with a high degree of difference between horizontal and vertical surfaces.

[0027] Figure 1D shows the result of etching the oxide 150 in a wet oxide etch such as dilute hydrofluoric acid or buffered hydrofluoric acid, to provide good control of the amount of material removed. The thin oxide on the interior walls of aperture 110 has been removed and the trench fill has been reduced to the height of layer 20 plus a process margin described below.

[0028] The dotted line labeled 155 represents the maximum amount of oxide that was put down. The area denoted with numeral 152 at the top of the pillars and the bottom

of the apertures represents the amount of trench oxide remaining after the etch.

[0029] Next, Figure 1E shows the result of etching the pad nitride 40, illustratively in hot phosphoric acid. Nitride 40 has been removed and isolated remaining portions of oxide 152 are shown as being removed. Numeral 157 denotes the new surface of the isolating oxide plugs in the isolation trenches. Those skilled in the art will appreciate that a margin has been left – i.e. that the surface of the isolation plug is above the level of the device layer 20. This is because further front end processing steps will remove some additional amount of oxide. The surface of oxide 155 in the trenches will be above the surface of layer 20 by a first margin (before etching oxide 155 from the walls) that is related to the thickness of the sidewall material. The first margin should be less than a reference amount such that the sidewall material can be removed. The height of the isolation plugs 157 of trench fill remaining after the wet etch will be above the height of layer 20 by a process margin set to allow for subsequent front end processes; i.e. such that the final height of the trench fill is substantially coplanar with the top of the device layer 20.

[0030] The preceding example has shown a simplified case in

which all the portions of nitride 40 are of about the same size. The wet etch is able to attack the nitride portions from both sides, for efficient removal.

[0031] In most integrated circuits, there will be at least some areas of silicon that have devices with wide active areas that need to be isolated. The nitride over those areas is too wide to be removed in a reasonable process time with the nitride etch.

[0032] Figure 2 illustrates a first alternative embodiment directed at a wide active area. Figure 2A illustrates the same initial structure as in Figure 1A. Substrate 5 is the bulk silicon, and BOX 10 supports SOI layer 20. Pad oxide 30 is present over the entire wafer, and pad nitride 40 completes the structure.

[0033] Figure 2B shows the result of etching an aperture down through the pad nitride 40 and pad oxide 30 and through the device layer 20, stopping on BOx 10.

[0034] Figure 2C shows the result of depositing a nonconformal oxide 155 in the trench and over the top of the pad nitride.

[0035] Figure 2D shows the result of depositing photoresist 210 over the wafer and patterning it to open an aperture 115 offset from the isolation aperture. The oxide beneath the

photoresist can be removed by any convenient process at an appropriate time. The new aperture (and others like it outside the area shown) are located over wide areas of pad nitride and close enough to apertures 110 to facilitate etching the nitride 40 from both sides.

[0036] Figure 2E shows the result of etching the isolation oxide 155, removing the oxide lining the walls of the isolation aperture and also exposing the pad nitride 40.

[0037] The exposed top surface of the pad nitride permits the phosphoric acid to penetrate into the body of the extensive slab of nitride in a way that is not possible without the extra apertures.

[0038] Figure 3 shows an alternative method of practicing the invention, in which the pad nitride over wide areas is weakened by ion implantation.

[0039] Figure 3A shows the same initial structure as Figure 2A, with substrate 5, having BOX 10 on it and device layer 20 above the box. Pad oxide 30 and pad nitride 40 complete the structure.

[0040] Figure 3B shows the result of forming aperture 110 through pad nitride 40, pad oxide 30 and device layer 20.

[0041] Figure 3C shows the result of partially depositing the trench oxide 150.

- [0042] Figure 3D shows the result of etching the trench oxide, leaving the desired plug in the trench (plus a margin to allow for further processing) and the residual amounts 152 on the top of pad nitride 40.
- [0043] Figure 3E shows the result of implanting ions such as Ge or As into pad nitride 40, prior to the nonconformal insulator fill. The implantation is denoted with the dashed line 160, indicating that the ions are implanted broadly and to a depth such that the ions in the tail of the implantation distribution have a concentration such that any penetration into the device layer does not have a significant effect on the transistors to be formed there.
- [0044] Figure 3F shows the result of the phosphoric acid etch of the pad nitride 40. The narrow pillar of nitride on the right of the figure has been removed, since it is attacked from both sides as in Figure 1.
- [0045] On the left of aperture 110, the etchant has penetrated laterally into pad nitride 40 in aperture 42.
- [0046] It is not necessary to have a blanket implant to facilitate pad nitride removal. The devices to be formed in the device layer may be sensitive to (and adversely affected by) the implant of the pad nitride. As a further option, an implant blocking mask may be used to cover and block the

areas of the wafer where the trenches are close together so that only the wide areas receive the implant.

[0047] The implant energy may be set to penetrate to the bottom of the pad nitride, so that the nitride is removed rapidly throughout its entire depth.

[0048] As a further alternative to this embodiment, both auxiliary trenches in wide field areas and implants may be used.

[0049] In all embodiments of this invention, the trench isolation is formed by undercutting the pad nitride, therefore megasonic cleaning or another particle removal technique is recommended to remove any residual oxide particles that may cling to the wafer as it is removed from the nitride etch solution. Megasonics are not strictly required to form the structure described in the invention, however they will assist with minimizing the number of defects, as known to those skilled in the art.

[0050] The oxide particles (residual HDP) are formed when the pad nitride is undercut because of the low etch rate of silicon dioxide in hot phosphoric acid. They will be present in the phosphoric acid during the pad nitride etch and may adhere to the wafer surface as the wafers are pulled out of the phosphoric acid. An additional clean to remove these particles is recommended to minimize defects.

[0051] Those skilled in the art will appreciate that various materials may be used according to the invention.

[0052] A preferred material for nitride 40 is plasma enhanced chemical vapor deposited (PECVD) nitride. This method of deposition produces a film that is etched much faster (about twice as fast) than standard low pressure chemical vapor deposited (LPCVD) nitride. Those skilled in the art are well aware of suitable parameters for these various methods, which will vary with the brand of deposition tool and are routinely tuned to suit a particular process.

[0053] A preferred method for the trench fill oxide is high density plasma deposition, which produces a relatively thin thickness on vertical surfaces.

[0054] As an example, a wafer may have a device layer thickness of from about 20 to 150 nm and a pad nitride thickness in the range of about 50 to 150 nm. The trench oxide fill may be from 35 to 300 nm, so that the first margin (distance of trench fill surface over device layer surface) can be from 15 to 150 nm and the process margin to allow for subsequent front end processing can be from 10 to 145 nm. This example is simply meant to demonstrate the wide process window for this invention. The appropriate values for these film thicknesses and process margins

should be chosen to match the design considerations and process flow of the product of interest.

[0055] Other integrated circuits and processes will have parameters differing from the foregoing in order to meet their requirements.

[0056] While the invention has been described in terms of several preferred embodiments, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

[0057] What is claimed is: